

What is claimed is:

- 1                   1.     A current steering circuit comprising:  
2                   a current input node coupled to a first circuit path, the first circuit path  
3 drawing current from the current input node during a first mode of operation;  
4                   a comparator coupled to the current input node, the comparator drawing  
5 negligible amount of current from the current input node during the first mode of  
6 operation, the comparator drawing significant amount of current from the current input  
7 node during a second mode of operation so as to divert current from the first circuit path;  
8 and  
9                   a current mirror coupled to the comparator, the current mirror maintaining  
10 current flow through a second circuit path during the second mode of operation but not  
11 during the first mode of operation.
- 1                   2.     The current steering circuit of claim 1 further comprising:  
2                   a reference node coupled to the comparator, the reference node providing a  
3 reference voltage;  
4                   a voltage input node coupled to the comparator, the voltage input node  
5 providing an input voltage; and  
6                   wherein the comparator places the current steering circuit in the first mode  
7 of operation or the second mode of operation when the input voltage is at a predetermined  
8 level relative to the reference voltage.
- 1                   3.     The current steering circuit of claim 1 further comprising a p-type  
2 differential amplifier coupled to a first circuit path, and an n-type differential amplifier  
3 coupled to a second circuit path.
- 1                   4.     The current steering circuit of claim 1 further comprising a current  
2 source coupled to the current input node.
- 1                   5.     The current steering circuit of claim 2 wherein the reference  
2 voltage is established by a diode-connected transistor.
- 1                   6.     The current steering circuit of claim 2 wherein the voltage input  
2 node includes an input terminal of a p-type differential amplifier.

1                   7.     A current steering circuit comprising:  
2                   a current input node coupled to a first circuit path, the first circuit path  
3 drawing current from the current input node during a first mode of operation;  
4                   a first transistor coupled to the current input node, the first transistor  
5 drawing negligible current from the current input node during the first mode of operation,  
6 the first transistor drawing current from the current input node during a second mode of  
7 operation to divert current from the first circuit path;  
8                   a second transistor coupled to receive current drawn by the first transistor  
9 from the current input node during the second mode of operation, the second transistor  
10 forming a current mirror with a third transistor that is coupled to a second circuit path;  
11                  a reference node providing a reference voltage to a fourth transistor;  
12                  a fifth transistor forming a current mirror with the fourth transistor, the  
13 fifth transistor supplying a reference current to the first transistor, the amount of the  
14 reference current being related to the reference voltage; and  
15                  wherein the current steering circuit is placed in the first mode of operation  
16 or the second mode of operation depending on a voltage level on a voltage input node  
17 relative to the reference voltage.

1                   8.     The current steering circuit of claim 7 wherein the current steering  
2 circuit is placed in the first mode of operation when the voltage level on the voltage input  
3 node is lower than the reference voltage, and in the second mode of operation when the  
4 voltage level on the voltage input node is higher than the reference voltage.

1                   9.     The current steering circuit of claim 7 wherein the current steering  
2 circuit is placed in the first mode of operation when the voltage level on the voltage input  
3 node is higher than the reference voltage, and in the second mode of operation when the  
4 voltage level on the voltage input node is lower than the reference voltage.

1                   10.    The current steering circuit of claim 7 wherein the first, second,  
2 third, fourth, and fifth transistors are MOS transistors.

1                   11.    A method for maintaining a substantially constant error in an  
2 output voltage sourced by an amplifier comprising a first circuit and a second circuit, said  
3 method comprising:

4 driving said output voltage in a first region of operation in each of said  
5 first circuit and said second circuit, wherein in said first region of operation, said first  
6 circuit substantially drives said output;  
7 sensing a condition wherein  $V_{in}$  reaches  $V_{ref}$ ; and  
8 causing a switch over from said first region of operation to a second region  
9 of operation in each of said first circuit and said second circuit, wherein in said second  
10 region of operation, said second circuit substantially drives said output;  
11 wherein  $V_{ref}$  is set to provide a substantially constant error within said  
12 output voltage.

1 12. The method of claim 11, wherein  
2 said first circuit is a p-channel amplifier and said second circuit is an n-  
3 channel amplifier.

1 13. The method of claim 12, wherein  
2 said first region of operation comprises operation wherein said p-channel  
3 amplifier is active and said n-channel is relatively not active; and  
4 said second region of operation comprises operation wherein said n-  
5 channel amplifier is active and said p-channel is relatively not active.

1 14. The method of claim 11, wherein  
2 said first circuit is a n-channel amplifier and said second circuit is an p-  
3 channel amplifier.

1 15. The method of claim 14, wherein  
2 said first region of operation comprises operation wherein said n-channel  
3 amplifier is active and said p-channel is relatively not active; and  
4 said second region of operation comprises operation wherein said p-  
5 channel amplifier is active and said n-channel is relatively not active.

1 16. The method of claim 11, wherein  
2  $V_{ref}$  is set to provide a substantially constant error within said output  
3 voltage by making  $V_{ref}$  sufficiently large in comparison to  $V_{in}$ .

1 17. The method of claim 11, wherein

2                   Vref is set to provide a substantially constant error within said output  
3 voltage by making Vref sufficiently small in comparison to Vin.

1                   18.     An apparatus, comprising:  
2                   means for driving an output voltage in a first region of operation in each of  
3 a first circuit and a second circuit;  
4                   means for sensing a condition wherein an input voltage (Vin) reaches a  
5 reference voltage (Vref);  
6                   means for switching over from a first region of operation to a second  
7 region of operation in each of said first circuit and said second circuit; and  
8                   means for setting Vref to be sufficiently large, thereby maintaining a  
9 substantially constant error in said output voltage.

1                   19.     A method, comprising:  
2                   driving an output voltage in a first region of operation substantially by a  
3 first circuit for a substantial portion of an amplifier's entire range of operation;  
4                   sensing a condition wherein an input voltage, Vin, reaches a reference  
5 voltage, Vref; and  
6                   switching over from the first region of operation to a second region of  
7 operation;  
8                   wherein a second circuit substantially drives the output voltage for a  
9 remaining portion of the amplifier's range of operation.

1                   20.     The method of claim 19, wherein  
2                   the reference voltage, Vref, is made sufficiently large to provide a  
3 substantially constant error within the output voltage by causing operation in the first  
4 region to occur for a substantial portion of the amplifier's entire range of operation.

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